Mask challenges in complementary EUV/193i patterning

Mark Phillips

Intel Corporation

Outline

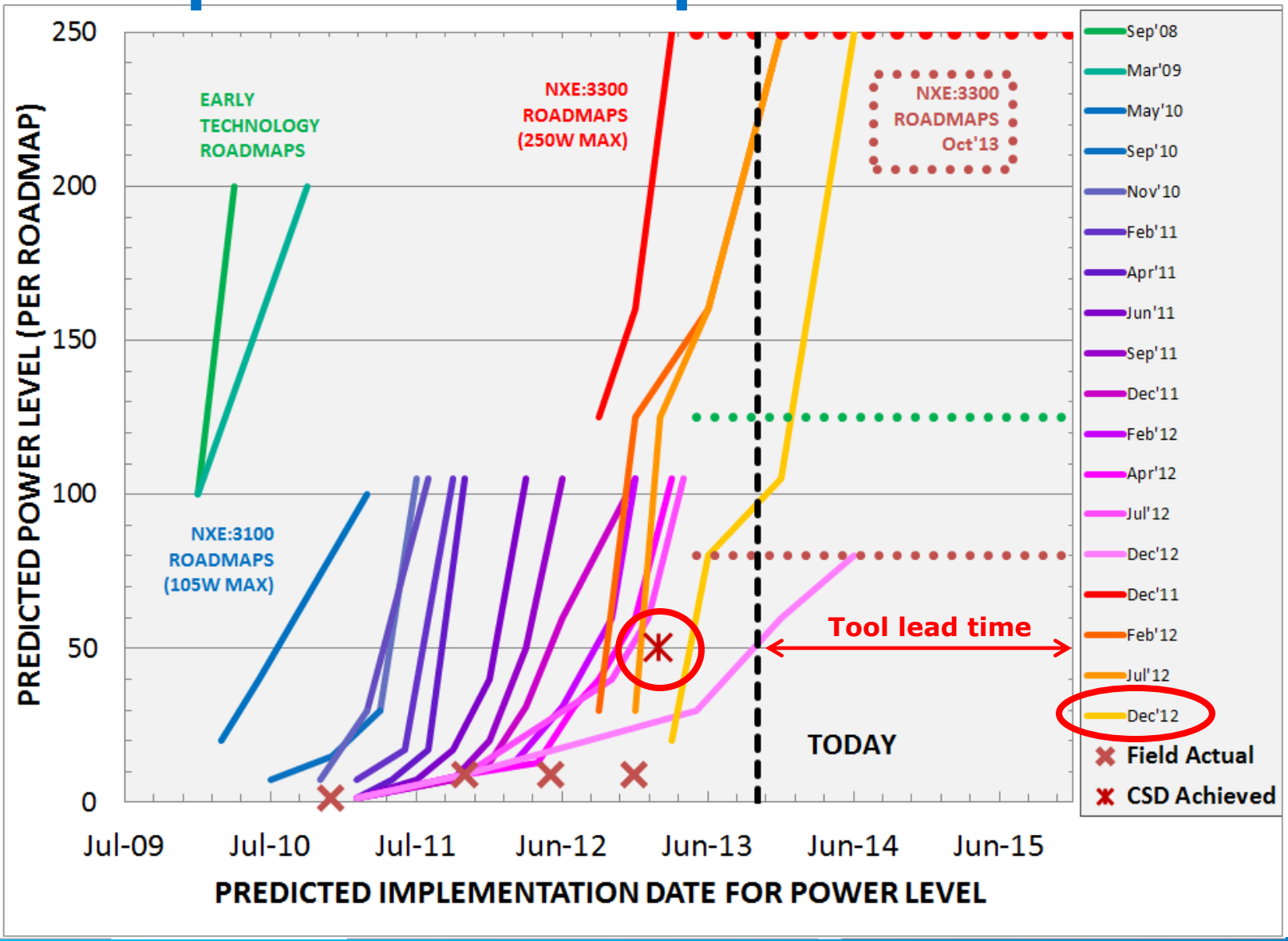
- EUV progress update
- Mask implications of EUV/193i complementary patterning
- EUV mask infrastructure

Problem Statement

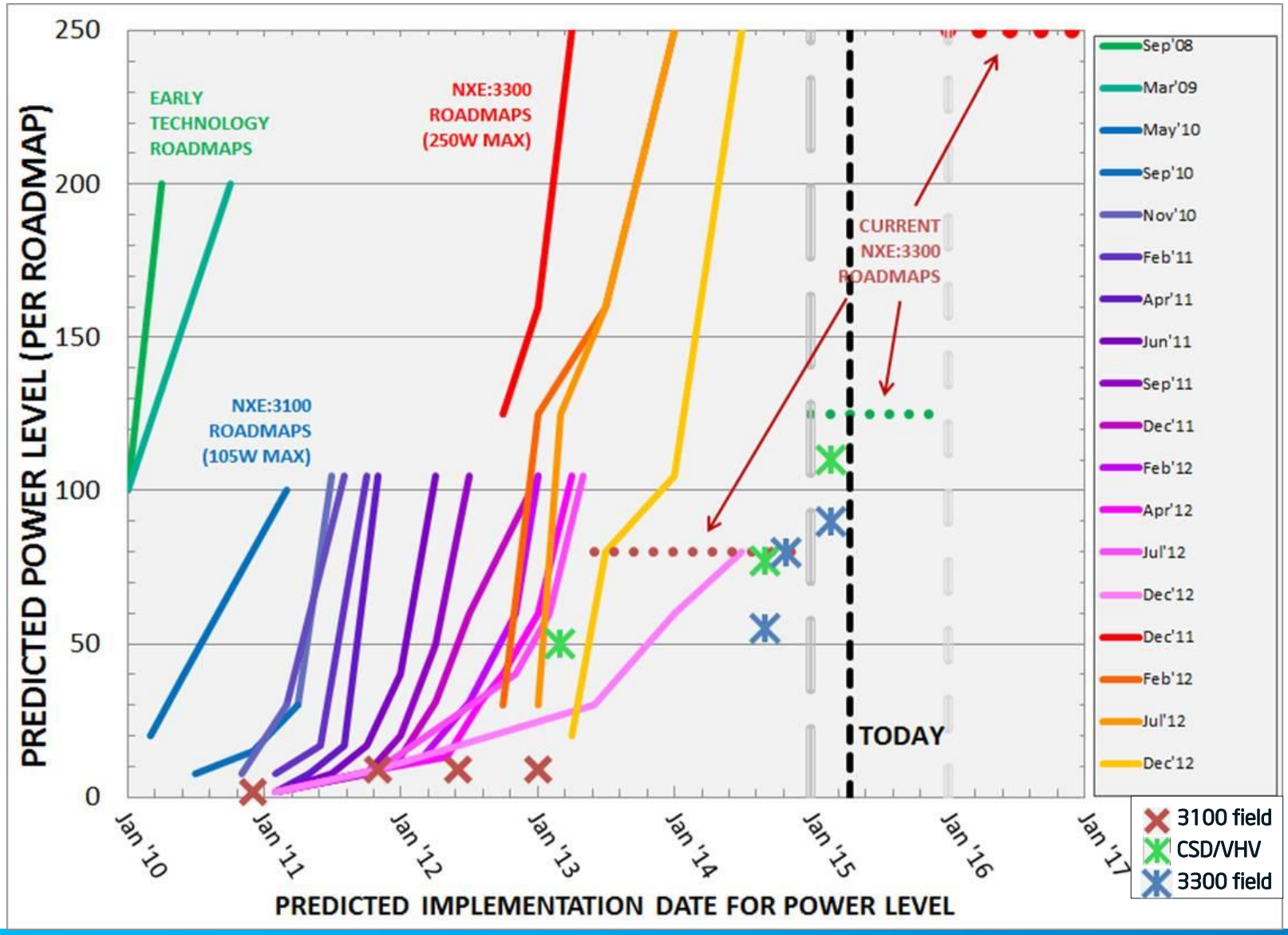
- Long delays in the exposure source power roadmap have undercut the credibility of EUVL
- Investments in other EUVL infrastructure have been reduced or delayed due to this uncertainty
- We are now at risk that practical power levels will be available before the complete infrastructure required for use of EUVL in HVM is ready.

As presented at 2013 Source Workshop

Source power roadmap has lost credibility



Two years of solid progress on source power



Worldwide fleet 40-80W

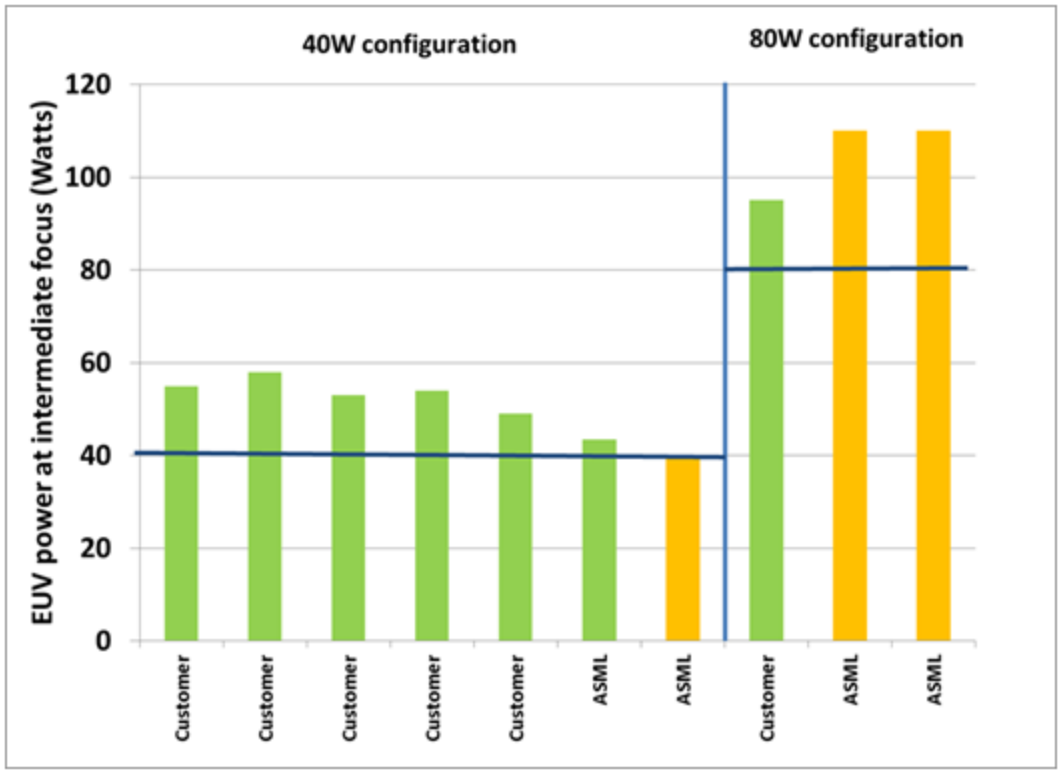
Multiple systems capable of >90W

All systems demonstrated capability to meet performance target

ASML

public

Slide 1



All results normalized to clean collector conditions

Slide courtesy ASML

Short-term productivity >1000wpd

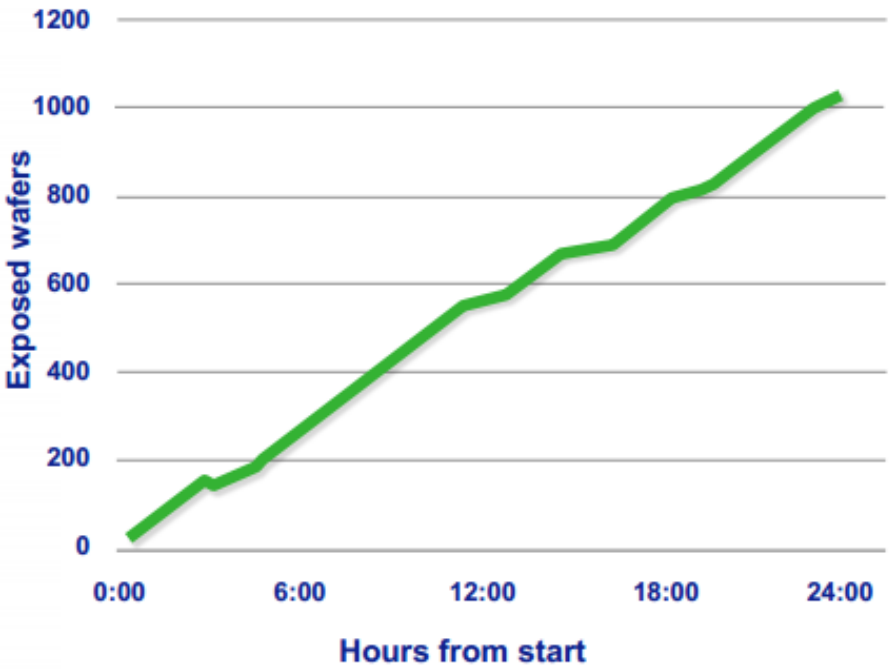
Today: 1,000 wafers per day capability demonstrated

On a field system, using customer exposure conditions, on 2 different days

ASML

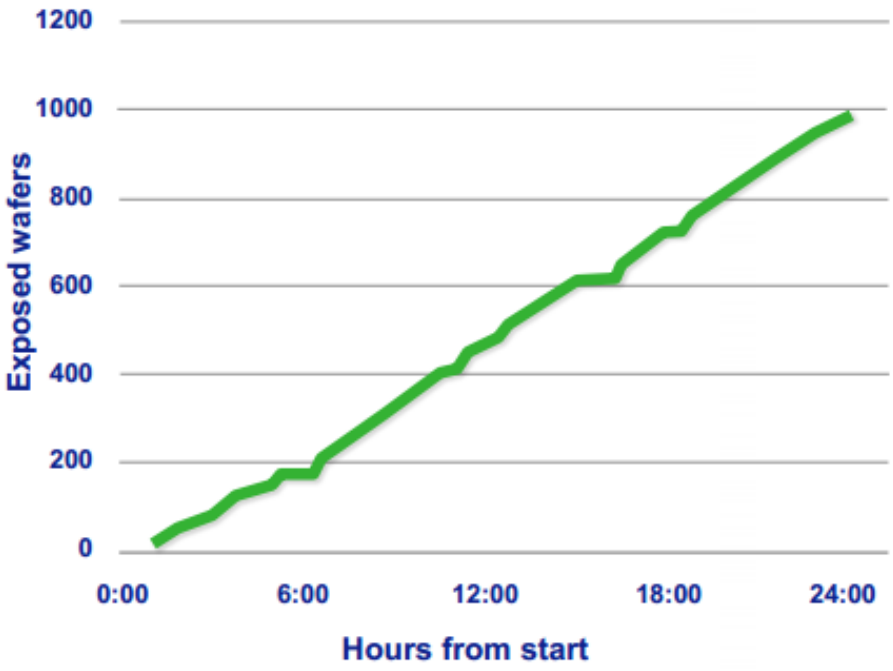
Public
Slide 5
February 2015

1,022 wafers exposed in 24 hours



80W source configuration

970 wafers exposed in 24 hours



Alberto Pirati, SPIE Advanced Lithography, 2015

What about exposure tool performance gates committing a process node to EUV?

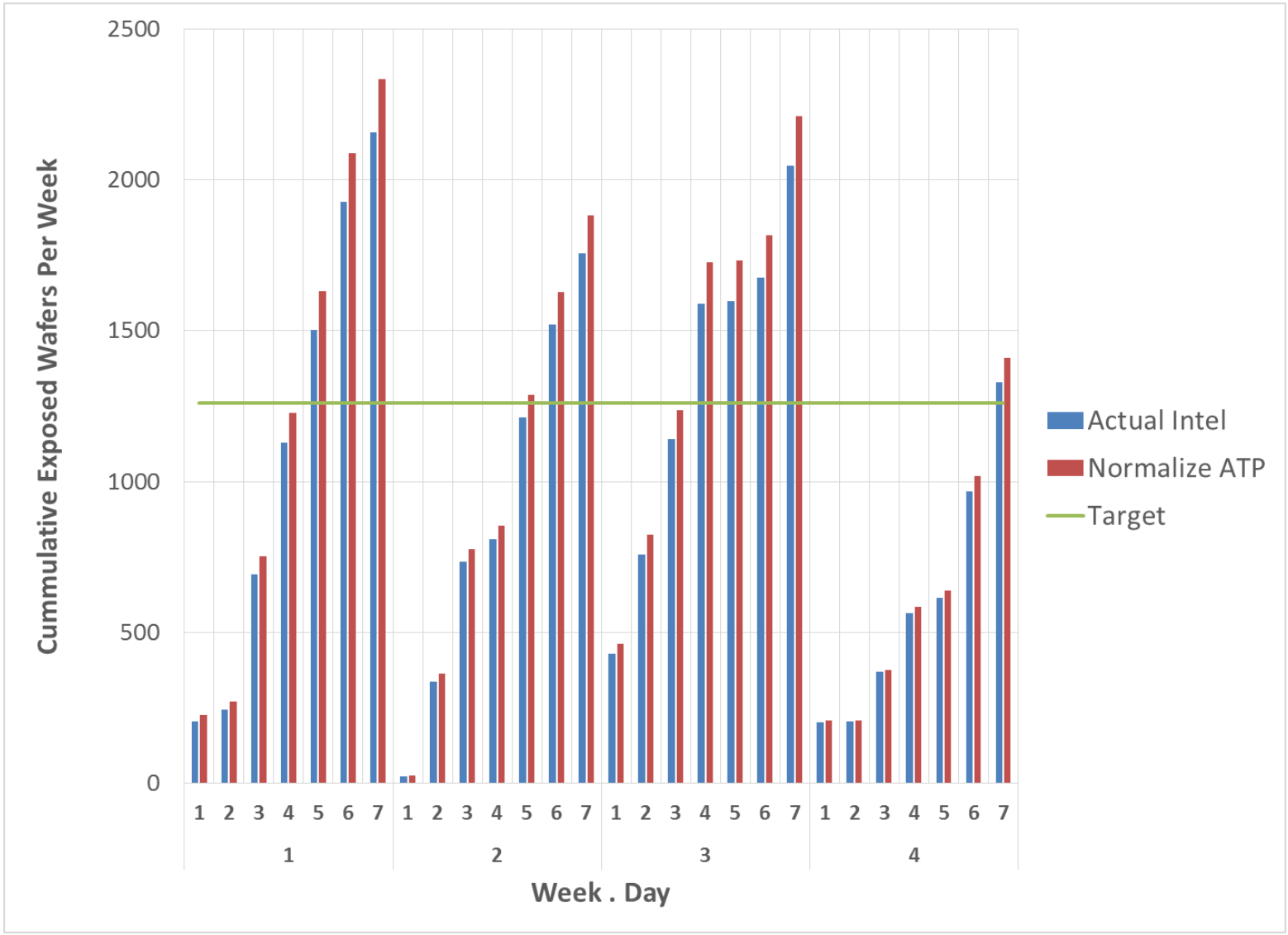
- Technology Development requires rapid information turns
  - Availability: tool must be up to run TD wafers without delay
- HVM requires reasonable COO and predictability, driven by:
  - Productivity (mostly source power)
  - Availability (mostly source availability)
  - OpEx (mostly source consumables)

Targets and results from 4-week demo

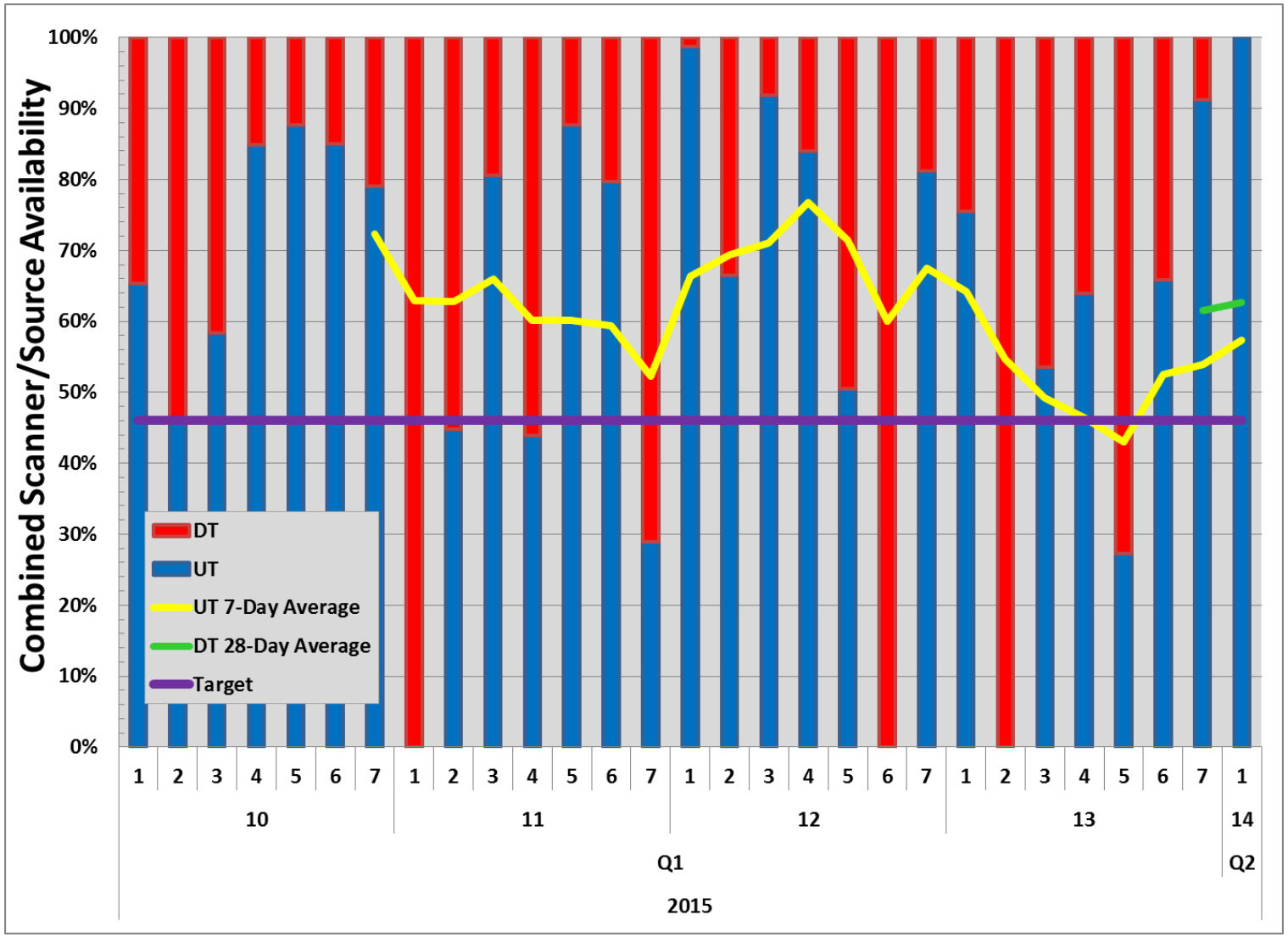
	Nominal Target	Demo-Time Adjusted Target	Result
Availability (scanner + source)	**46%**	**46%**	**61%**
TPT - good wafers per day	**180**	**170**	• **280** normalized WPD • ***260*** actual exposed WPD (raw count)
TPT - good wafers per week	**1260**	**1189**	• **1959** normalized WPW • ***1822*** actual exposed WPW (raw count)
No consecutive DT > 72hrs	**<72hrs**	**<72hrs**	Max consecutive downtime = **36hrs** (DG swap + Sn catch drain + RF generator failure/replacement on PA0)

- Goal: demonstrate tool can run as advertised for 40W config today
- Targets based on 125 fields/wafer at 15mJ/cm^2 dose
- Actual wafers exposed were a variety of shot maps and doses, so "normalized" count converts to equivalent at 125 fields/15mJ
- Integrated test-chip wafers allowed verification of imaging, overay, and defects throughout demo → results all good

Demo cumulative wafers per week

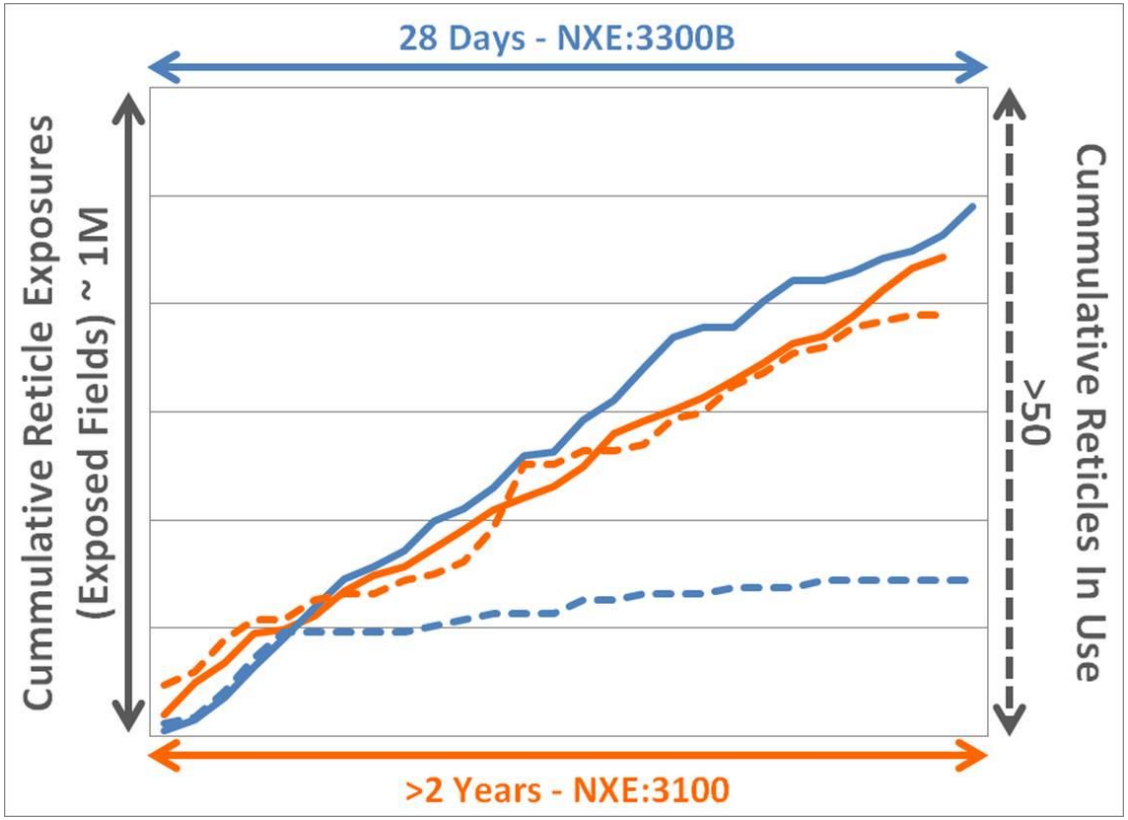


Demo availability (4 weeks)



- Far from OK for production, but better than expected for current 40W config

NXE:3300 accelerating learning on EUV reticle usage



- > 300 reticles associated to NXE scanner platform fabricated since 2010
- The NXE reticles are closely monitored in their functionality, reliability and utilization.
- Several plates, each utilized over 2 years, exposed to >10kJ EUV irradiation
- NXE:3300B now allows study with higher-power and throughput
- Only experience with pellicles in place was demonstration with full-size proto pellicle

Summary of EUVL status

- Two years of solid progress on EUVL
  - Eight 0.33NA systems shipped, generally meeting all performance specs not related to source power
  - 40W, 80W, now 100W (@IF) MOPA/PP demonstrated in the field
  - ~500wpd, then ~1000wpd in short-term (1-2 day) demonstrations
  - 4 week demonstration of availability, output, imaging and overlay consistent with 40W tool configuration
- Introduction in production is a question of "when" rather than "if"
  - Availability, stability and operating cost are still concerns
  - Need to ensure infrastructure does not gate HVM

Outline

- EUV progress update
- Mask implications of EUV/193i complementary patterning
- EUV mask infrastructure

How will EUV be used at introduction?

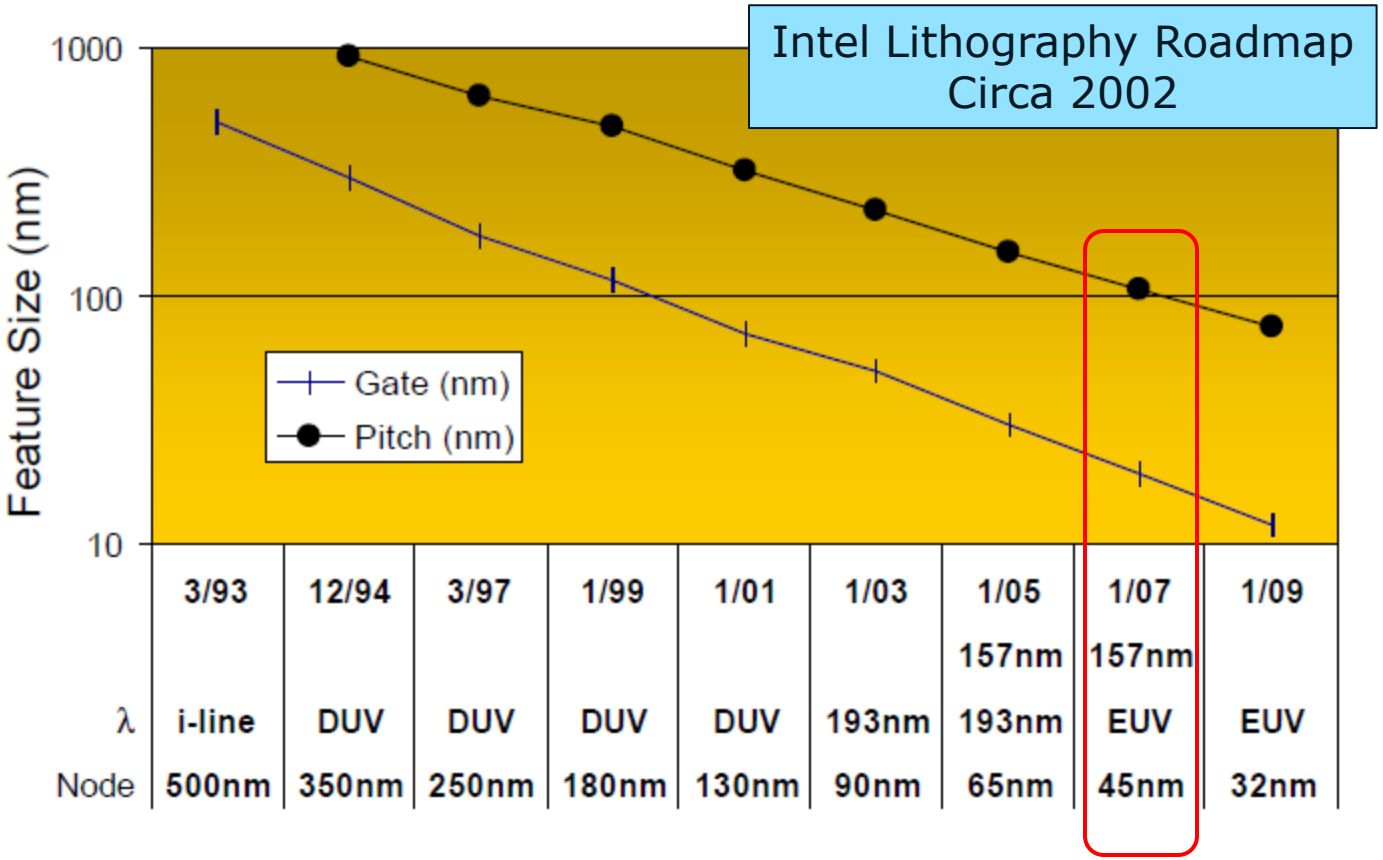


Figure 1: Intel Lithography Roadmap

Plan A: Insertion as high-k1 single exposure

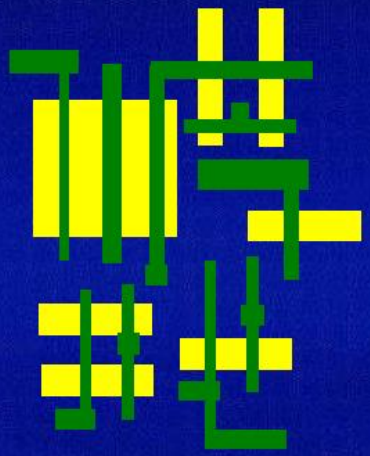
OK, so what is Plan B?

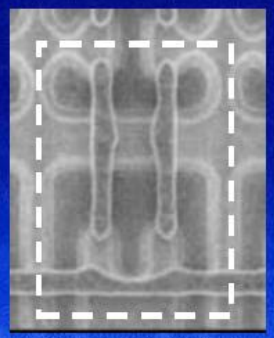
A lot has happened in 13 years…

Process Friendly Design Rules Gradually Implemented

90nm

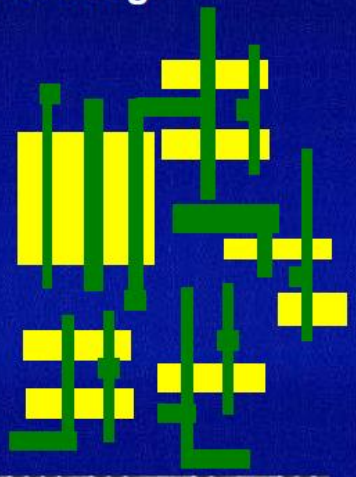
- All gates in one direction except SRAM.

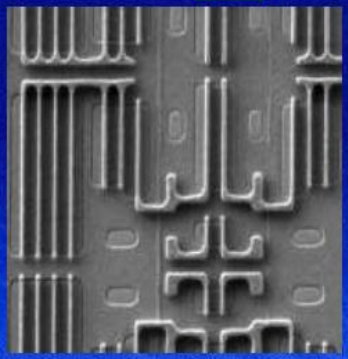




65nm

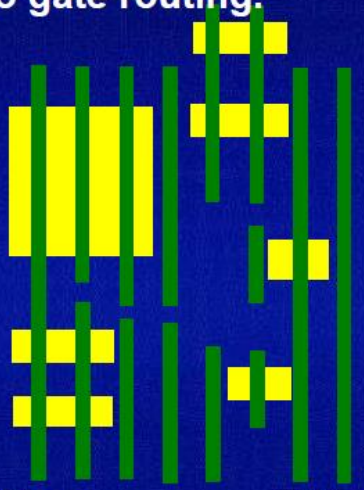
- All gates in one direction everywhere.
- Different rules for minimum pitch, larger gate pitch and gate routing.



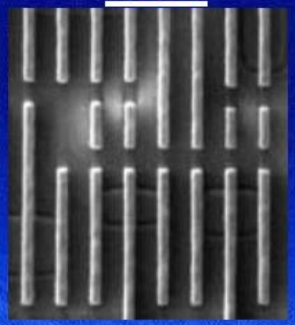


45nm/32nm

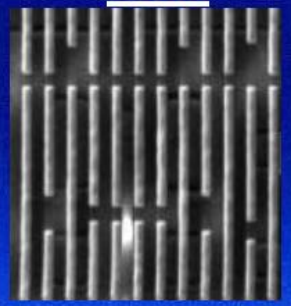
- All gates in one direction and one pitch.
- Trench contact local routing replaces orthogonal to gate routing.



45nm



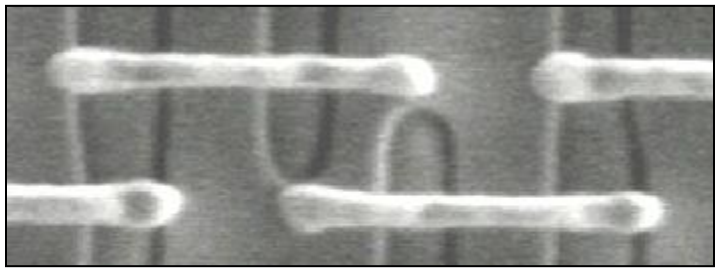
32nm



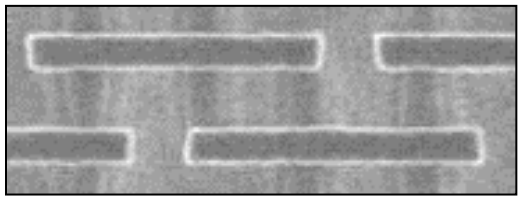
Schenker, CICC 2013

Restricted DR & grating/cut are here to stay

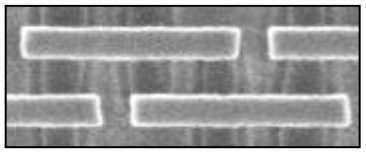
SRAM cell scaling



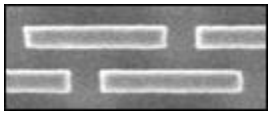
65 nm, 0.570 um^2



45 nm, 0.346 um^2



32 nm, 0.171 um^2



22 nm, 0.092 um^2

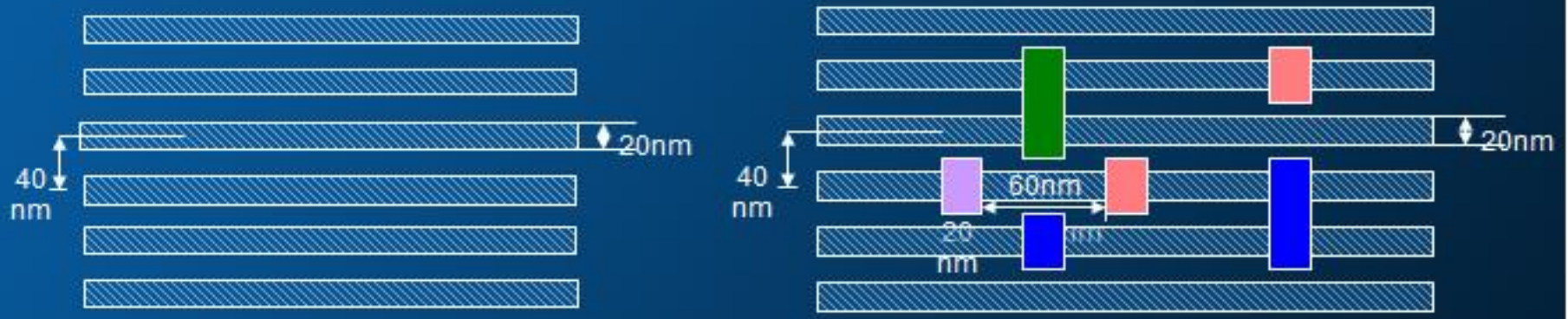
grating+cut litho

- Gradual introduction of stricter DRs was density-neutral or better
- Improved control of features beneficial to device performance and yield
- These layouts are here to stay, regardless of the exposure wavelength
- Only question is optimal techniques for doing gratings and cuts

"Complementary" patterning proposed by Yan Borodovsky ~2010

20[illegible] Node

ArF Only Patterning



1 193i w/PD to form gratings + 4 193i Masks/Exposures to form Pattern = 5 Mask 5 Exposures

Complementary Patterning

CDU, LWR <2nm 3s

CDU, LWR <4nm 3s

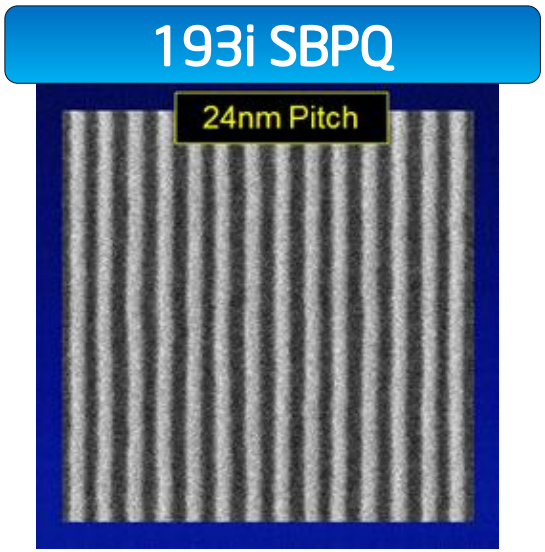
1 Mask/1 193i Expose + 1 Mask/1 EUV Expose or 0 Mask/1 EBDW Expose

1 193i w/PD to form gratings + 1 EUV Masks/Exposure or 0 Mask/1 EBDW Exposure
Total 2 Masks/2 Exposures or 1 Mask/2 Exposures

Yan Borodovsky, KLA-Tencor LUF, Feb.21st 2010, San Jose , Ca, USA

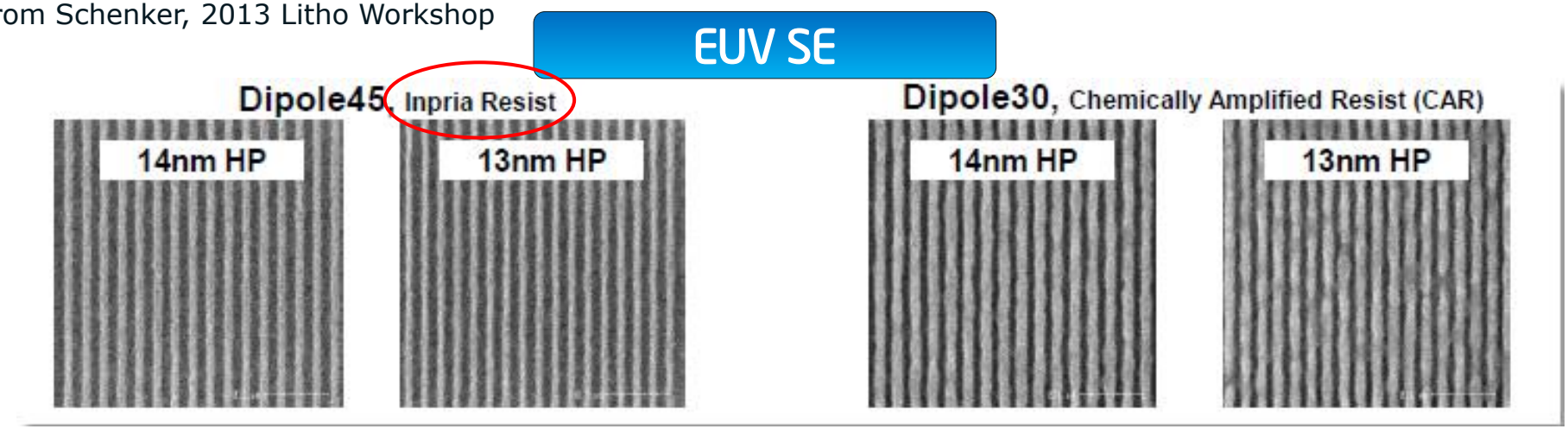
20

Optimal choice for grating



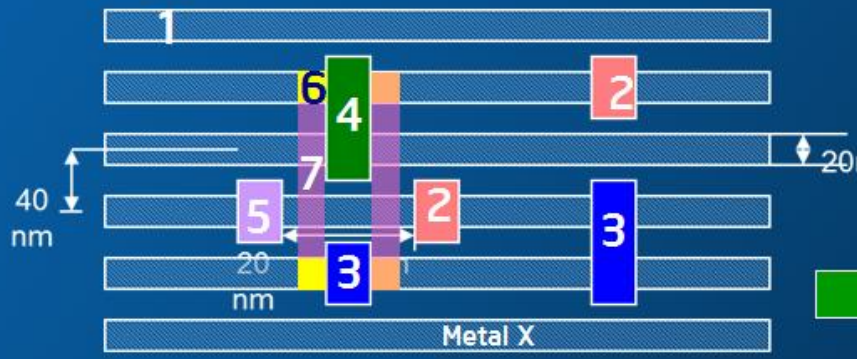
From Schenker, 2013 Litho Workshop

- Today, 193i + SBPQ is the better option for grating (~1/3 cheaper than EUV)
- In long term, need to quantify full EPE budget for each option (LER, MMO, "pitch walking", spacer variability) and reconsider for mature EUV power and CoO

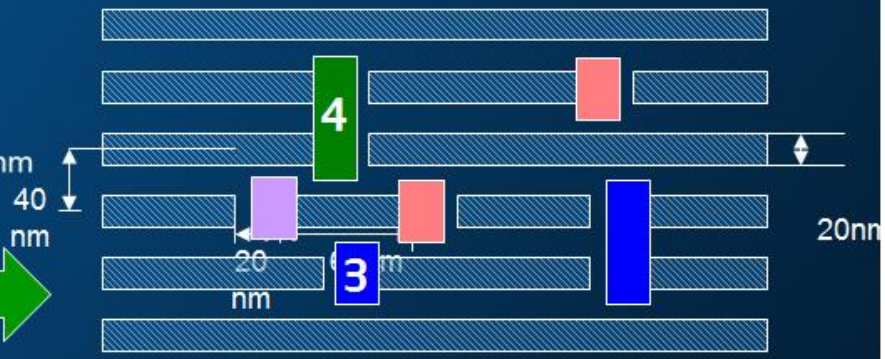


From Brandt *et al.*, EUVL Symposium, 2013

Cut/Via/Metal Non-Scaling Overlay is ultimate limit to amount of Cut and Via split masks

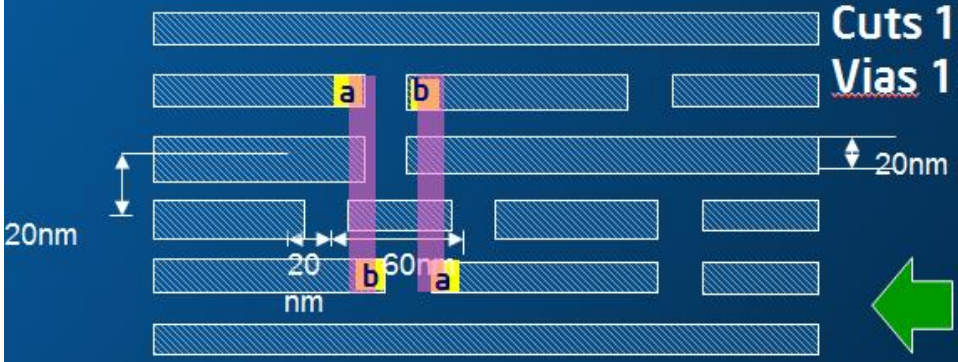


Design: #2-#5 Cuts, #6 Vias, #7 Mx+1

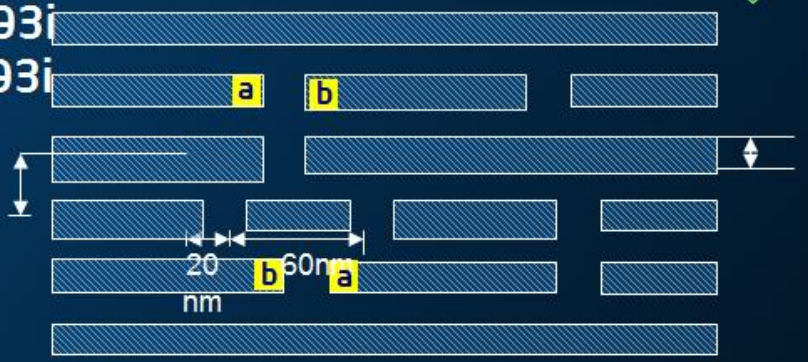


Cuts Printed with some OL errors

Cuts 193i
Vias 193i



Whichever Via mask one aligns
Metal x+1 to there is a problem



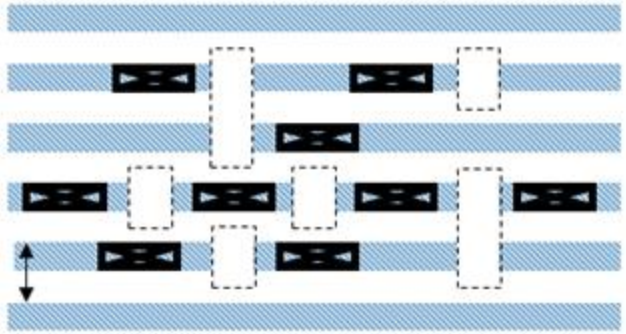
Vias "a" aligned to Cut Mask #3&#4
Vias "b" aligned to Cut mask #3&#4

This is Ultimate limit to Over-scaling with Pitch Division

Y.Borodovsky, Alternative Lithographic Technologies VII, Conference 9423, 23 February 2015, San Jose, CA, USA

20

EPE & cost drive Complementary EUV/193i



- EPE budget ultimately limits scaling of layout
- Grating/cut is still optimal for metal layout. Note: only one tight alignment in each direction.
- Critical issue for EPE is keeping all cuts on one mask and all vias on one mask. Resolution of EUV allows this with cost parity at ~1:3 EUV:193i
- 193i + n * SPD can create gating at ~1/3 cost of EUV at 250W

What does complementary EUV/193i mean for mask makers?

- Introduction of EUV slows increase in mask count.
- 193i layers are part of EPE budget for critical process features
  - Requires improved 193i overlay and CDs, including mask contributions
- 1 EUV mask will have features from 3-4 193i masks, so data will be large, and features will be small
  - Need data handling for larger files (perhaps some benefit from reduced OPC feature complexity at insertion, but flare compensation flattens data)
  - Small features drive reduced resist sensitivity
  - Write times increase → need multi-beam patterning

Complementary EUV/193i requires tight EUV/193i mask registration

- Need tightest possible mask registration control
- Non-telecentricity of EUV optics on mask side requires improved substrate flatness
  - 30nm PTV spec vs 150-200nm for 193i
  - Current performance ~50nm. 30nm probably doable with some yield loss
- Must correct all systematic EUV/193i mismatches
  - Account for gravity sag, chuck and pellicle stress during writing, metrology and use on scanner
  - Pattern-up kinematic during write and metro; pattern-down vacuum clamp at edge on 193i scanner; pattern-down e-chuck on EUV scanner

write/metro

193i vacuum clamp

EUV e-chuck

Outline

- EUV progress update
- Mask implications of EUV/193i complementary patterning
- EUV mask infrastructure

EUV Infrastructure Readiness Snapshot

EUV infrastructure has 8 key programs

1 is ready now, 4 are in development, 3 have significant gaps

E-beam Mask Inspection: HVM capable tool exists

AIMS Mask Inspection: SEMATECH-led tool development program

Actinic Blank Inspection (ABI): EIDEC-led tool development program

Pellicle: ASML commercializing

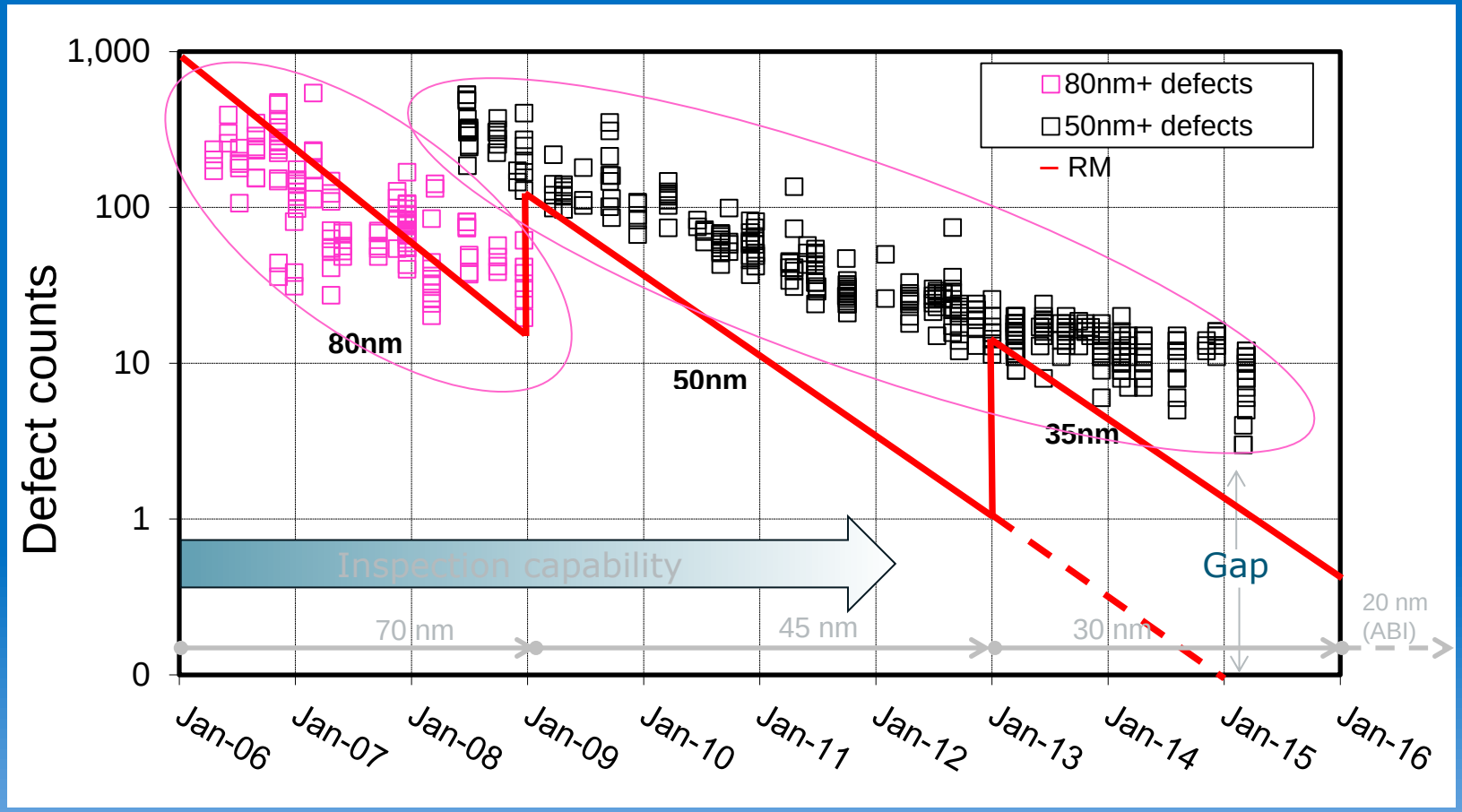
EUV blank quality: Process and yield improvements ongoing

Post-pellicle mask inspection: APMI not on timeline for insertion. Need other options.

Blank multi-layer deposition tool: Improving defect results. Multiple deposition techniques being evaluated to define HVM tool approach.

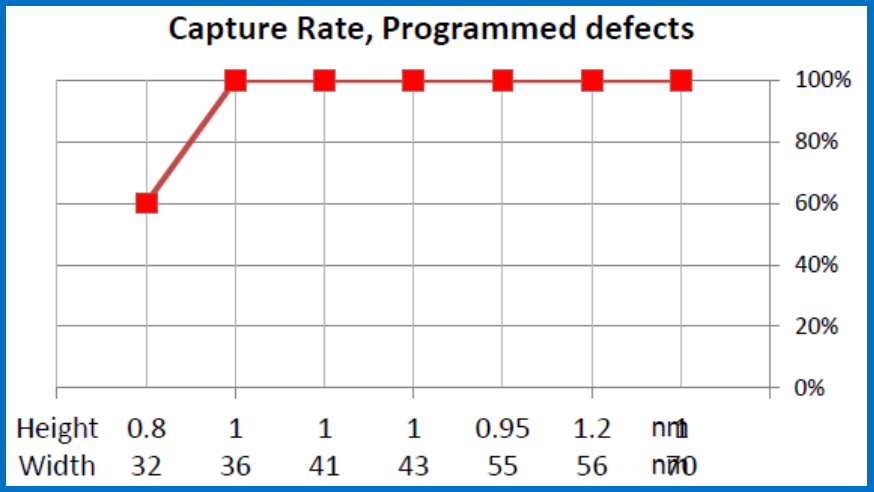
EUV resist QC: Industry-wide QC center finalizing definition

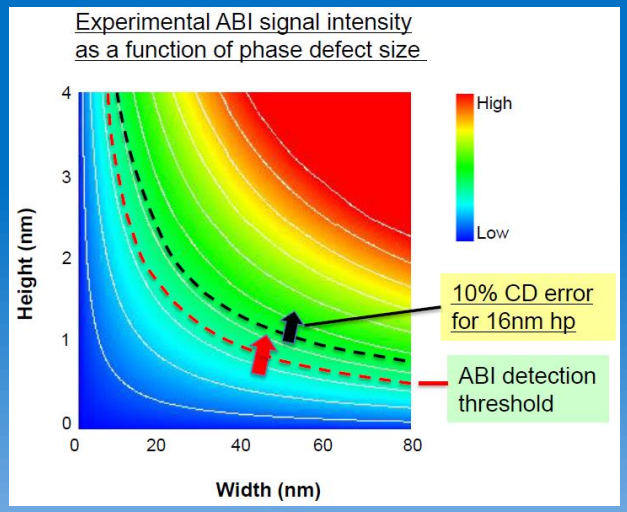
EUV mask blank ML defect trend

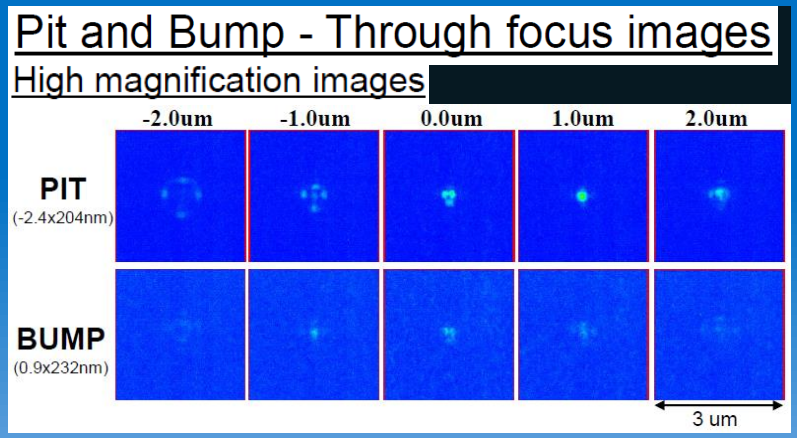


- EUV blanks with single digit (ML) defect count at 50 nm become commercially available
- Gap to the RM still needs to be closed for HVM
- Advanced inspection capability is required for further defect reduction

ABI Tool Development at EIDEC/Lasertec

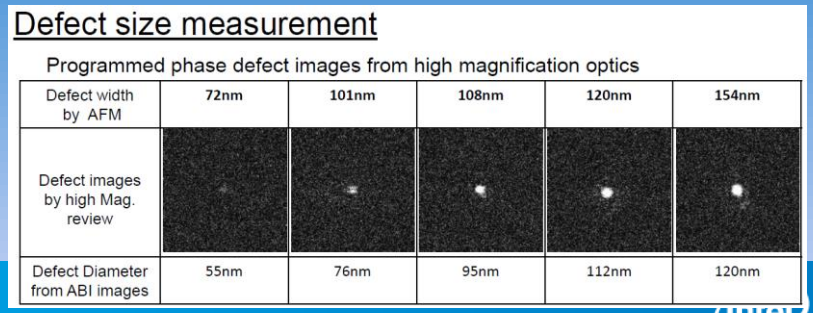






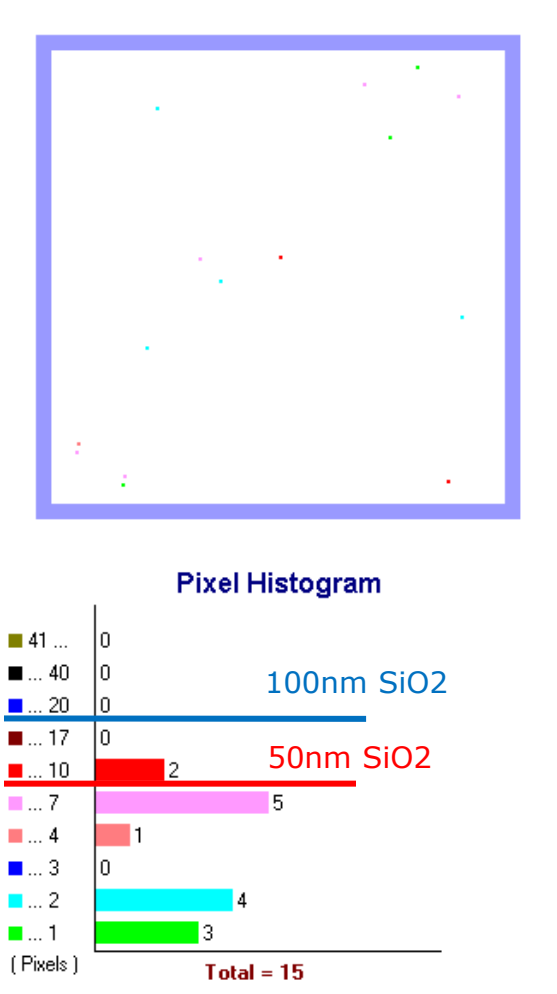
- LT-ABI HVM prototype is designed to detect 20nm defect with Phase/Amplitude and Pit/Bump classification

  - Reported at 2014 EUV Symposium by Lasertec

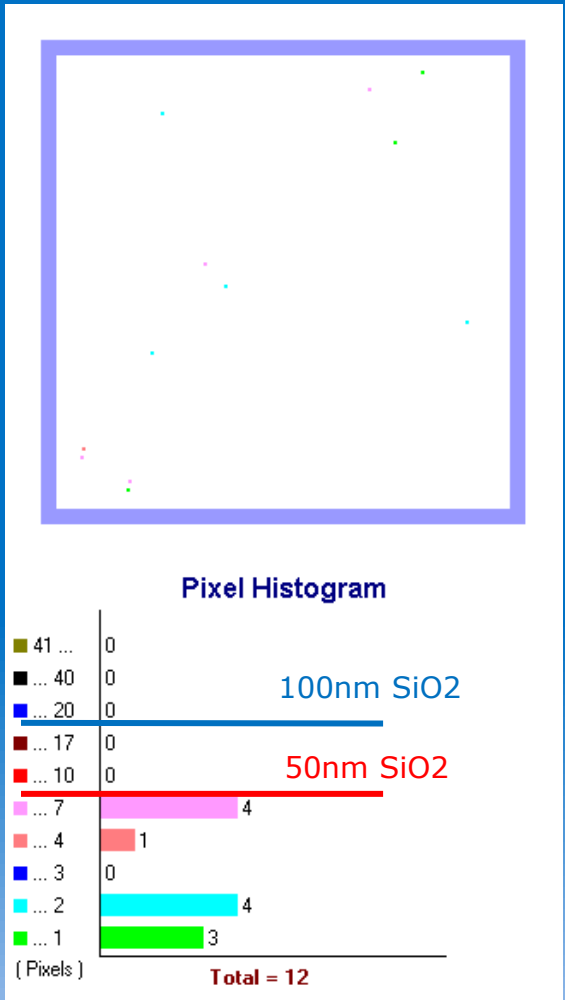


AGC EUV blank ML defect map

Q4/14 ML Blank Total defects



Q4/14 ML Adders



Slide courtesy AGC

Blank defect / mitigation summary

- Blank defect trend at 50nm solidly in single-digit range, making mitigation effective
- ABI in regular use, allowing sampling at 20nm SEVD
- Champion blanks approaching single-digit defects with ABI inspection
- ABI defect location accuracy approaching 10nm target
- Still need engineering work to define blank fiducial strategy compatible with low defects and placement accuracy

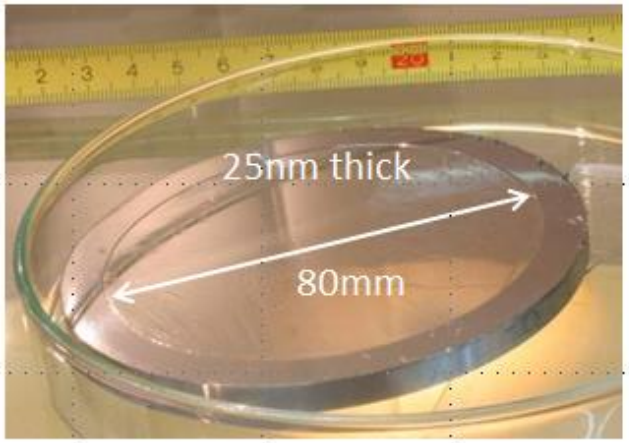
Membranes as of February 2013

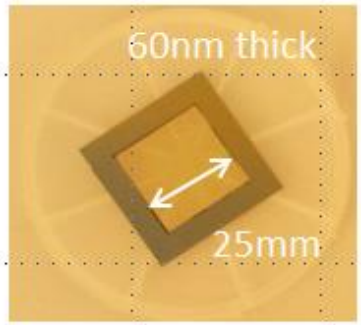
As presented at 2013 ASML Technology Symposium

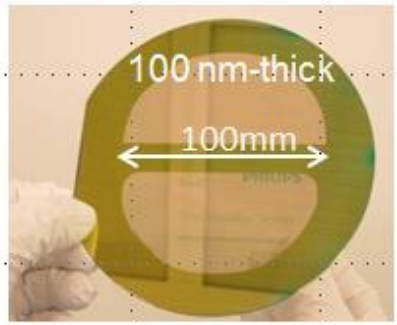
Free-standing pellicle can be manufactured on large areas

ASML

- ASML is investigating several materials, including:
- **Multilattice Pellicle**
  - Si/Mo/Nb-based multilayer
  - Free-standing : no support grid
  - Status
    - 86% EUV transmission
    - 20-25nm thickness
    - 80mm diameter
- **Poly-Silicon Pellicle**
  - Manufactured from standard silicon wafers using standard semiconductor manufacturing process
  - Free-standing : no support grid
  - Status:
    - ~ 80-82% EUV transmission
    - 60nm thickness
    - 25x25mm^2 area
    - Size up to 100x50mm (100nm thick)



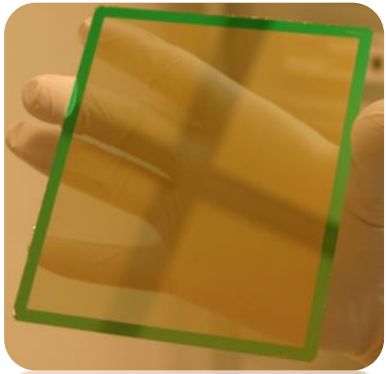




Foil shown in 2013 courtesy ASML

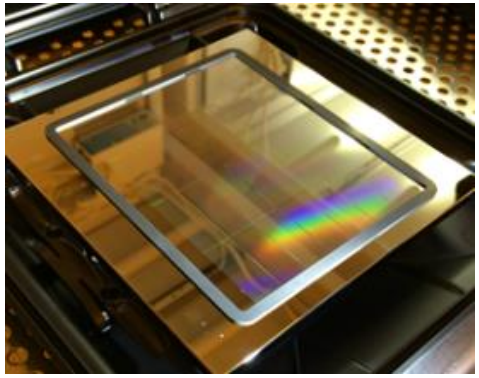
Wafers successfully exposed in NXE:3100 with a full-size prototype pellicle

Full size prototype film



103mm x 122mm (~85% EUV transmission)

Full size prototype frame mounted to reticle



Full size prototype frame and film mounted to reticle

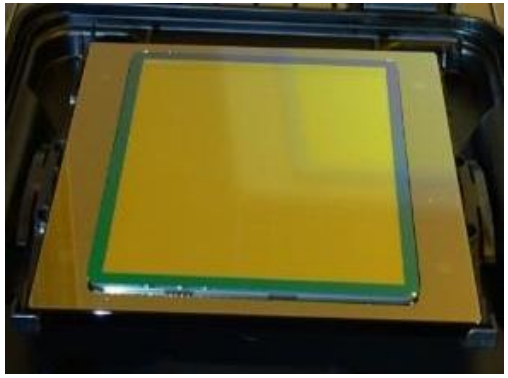
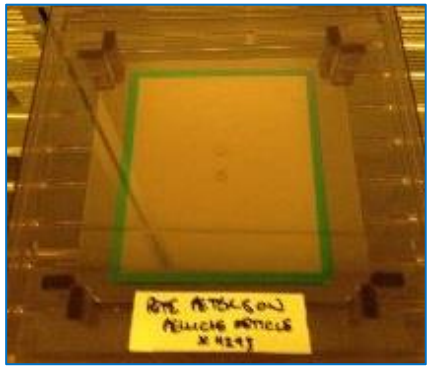


Image and mechanical testing of full size prototype pSi pellicles completed

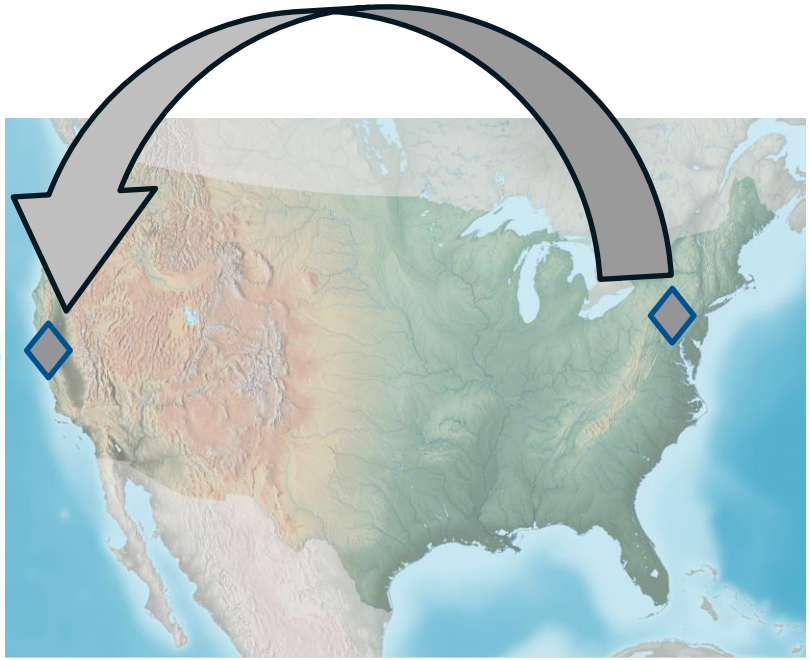
Pictures courtesy ASML, as shown by Sang Lee at Semicon Korea 2015

ASML

pSi Membrane is Robust



Regular shipping box



intel

ASML Wilton

Pelliclized reticle shipped across the US with the film intact.

Pictures courtesy ASML, as shown by Sang Lee at Semicon Korea 2015

EUV reticle inspection roadmap prior to EUV pellicle feasibility

Original industry plan for EUV reticle inspection:

- Extend ArF inspection
- Use e-beam inspection as low-productivity bridge
- Develop Actinic (13.5nm) Patterned Mask Inspection (APMI) tool for sensitivity and productivity

But…

- Neither e-beam nor ArF can inspect through pSi pellicles
- Development of APMI stalled due to high-cost and long lead time (~4 years?)

Proposed alternatives to APMI

- Make EUV scanner so clean a pellicle is not necessary
- Make pellicle mounting perfectly clean **and** hope nothing happens to pattern under pellicle
- Inspect through pellicle with long wavelengths
- Use Patterned Wafer Inspection (PWI) to detect repeating defects
- Accept the cost of yield loss due to repeating defects

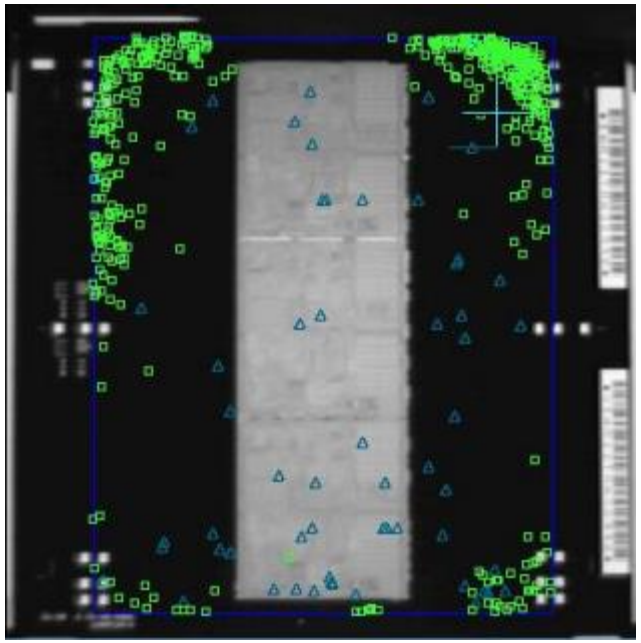
Proposed alternatives to APMI

- Make EUV scanner so clean a pellicle is not necessary→continue to pursue, but highly unlikely to be sufficient
- Make pellicle mounting perfectly clean **and** hope nothing happens to pattern under pellicle
- Inspect through pellicle with long wavelengths
- Use Patterned Wafer Inspection (PWI) to detect repeating defects
- Accept the cost of yield loss due to repeating defects

Make pellicle mounting perfectly clean and hope nothing happens to pattern under pellicle

- 365/248/193nm pellicle mounting is not perfectly clean after decades of work by mask shops.
- Various photo-induced defect (PID) mechanisms have plagued 193 masks for >10 years.
- PID mechanisms in vacuum with 13.5nm photons are unknown.
- Area under pellicle will not be purged and will contain outgassing from pellicle frame and adhesives

PID growth on Intel 193 mask

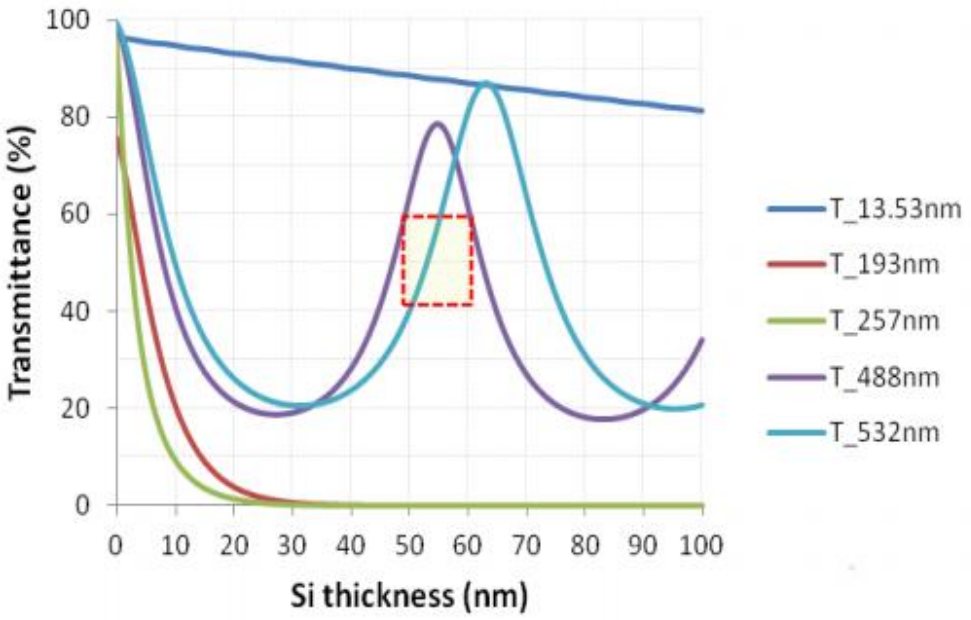


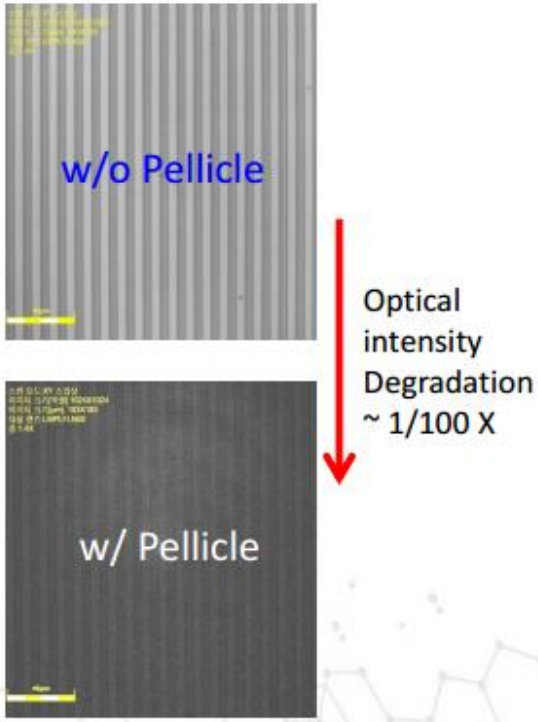
Eschbach *et al.* Proc. of SPIE Vol. 5853

Proposed alternatives to APMI

- Make EUV scanner so clean a pellicle is not necessary→continue to pursue, but highly unlikely to be sufficient
- Make pellicle mounting perfectly clean **and** hope nothing happens to pattern under pellicle→based on >10 years of 193 experience, this is unlikely, and we can't wait to find out
- Inspect through pellicle with long wavelengths
- Use Patterned Wafer Inspection (PWI) to detect repeating defects
- Accept the cost of yield loss due to repeating defects

Thru pellicle inspection





From Byung Gook Kim, SEMICON Korea 2015

Through-pellicle inspection at long wavelengths

- For particle detection without resolving the patterns on the mask surface, sensitivity is about 0.35um @488nm *with no pSi pellicle in place*
- 94% of fall-on particles found on EUV reticles used in EUV tools at Intel are <300nm and would not be detected @488nm even without optical impact of pSi pellicle
- With EUV pellicle in place, sensitivity will be significantly worse (exact value TBD)
- Required sensitivity ~30nm

Proposed alternatives to APMI

- Make EUV scanner so clean a pellicle is not necessary→continue to pursue, but highly unlikely to be enough
- Make pellicle mounting perfectly clean **and** hope nothing happens to pattern under pellicle →based on >10 years of 193 experience, this is unlikely, and we can't wait to find out
- Inspect through pellicle with long wavelengths→not useful for observed particle distribution or detecting PIDs before they impact imaging
- Use Patterned Wafer Inspection (PWI) to detect repeating defects
- Accept the cost of yield loss due to repeating defects

Use Patterned Wafer Inspection (PWI) to detect repeating defects

Idea:

- Print wafer with reticle under test
- Inspect with patterned-wafer inspection tool
- Filter for defects appearing in more than N fields

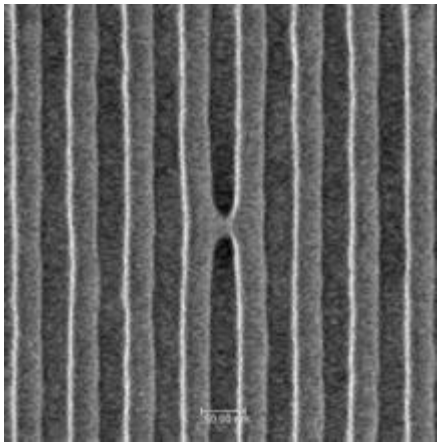
Consider:

- Printing with 13.5nm light
- Inspecting with dry DUV optics at 1X (that is, wafer level)

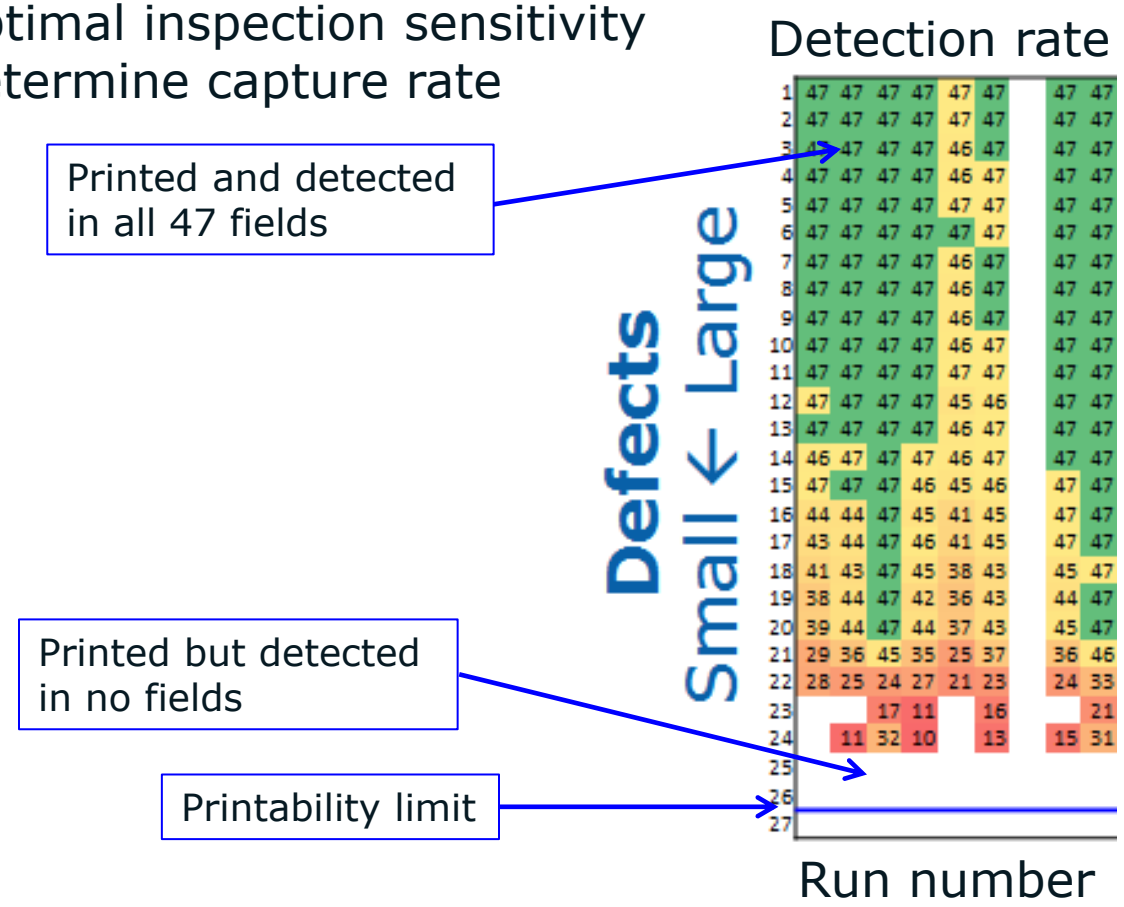
What do you expect to happen?

Example of limitations of PWI for reticle inspection

- 32/32 L/S reticle with Programmed Defect Array
- Exposed on TW for optimal inspection sensitivity
- Exposed ~ daily to determine capture rate



Example SEM image of programmed defect as printed on wafer



PWI conclusions

- Misses small defects even on line/space patterns on test wafers, where inspection tool has best sensitivity
- Detection of single missing vias is much more difficult, as is detection on product wafers
- Measured distribution of particles on EUV masks at Intel shows majority of defects will be small (e.g. impact to single via)
- Not useful for tracking PID growth
- Would require much higher resolution inspection than current DUV optical

Proposed alternatives to APMI

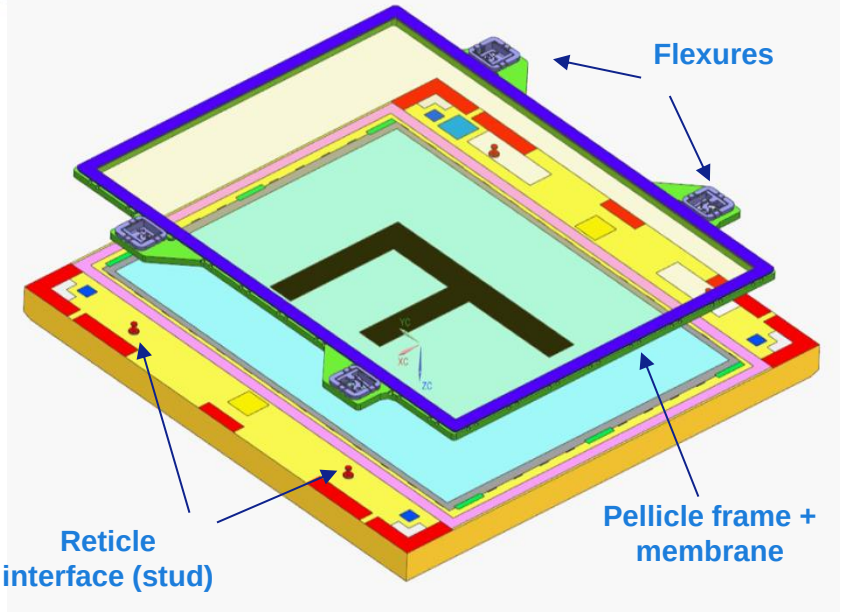
- Make EUV scanner so clean a pellicle is not necessary→continue to pursue, but highly unlikely to be sufficient
- Make pellicle mounting perfectly clean **and** hope nothing happens to pattern under pellicle→based on >10 years of 193 experience, this is unlikely, and we can't wait to find out
- Inspect through pellicle with long wavelengths→not useful for observed particle distribution or detecting PIDs before they impact imaging
- Use Patterned Wafer Inspection (PWI) to detect repeating defects→will be used for partial containment, but not capable of full containment
- Accept the cost of yield loss due to repeating defects→OK in TD. Only option in HVM until APMI is available, but cost and disruption to good-die-out will be painful.

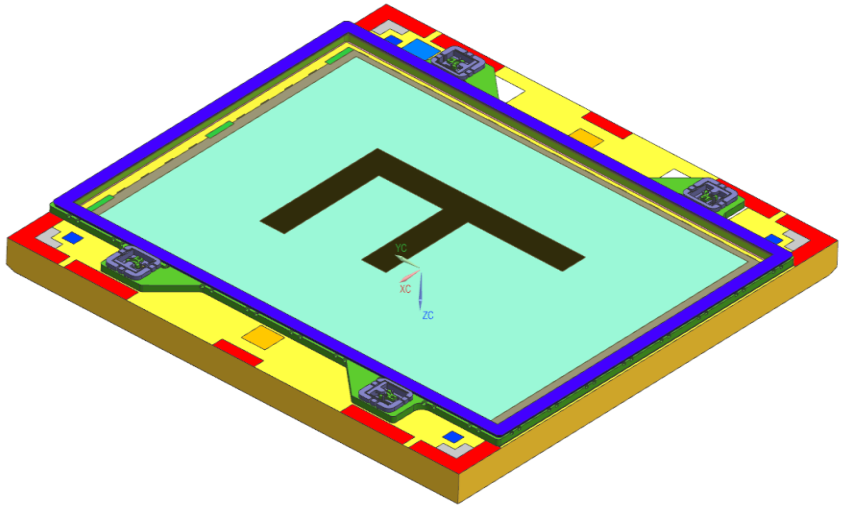
APMI conclusions

- EUV pellicles are feasible, but need to be commercialized
- Through-pellicle inspection is the industry standard, and the only known way to guarantee integrity of a pattern under a pellicle
- Delivery of APMI should not gate progress on EUV introduction, but we can't wait to start ~4yr development project
- APMI development needs to start now and occur in parallel with EUV introduction

Interchangeable NXE Pellicle concept

Allowing multiple inspection schemes





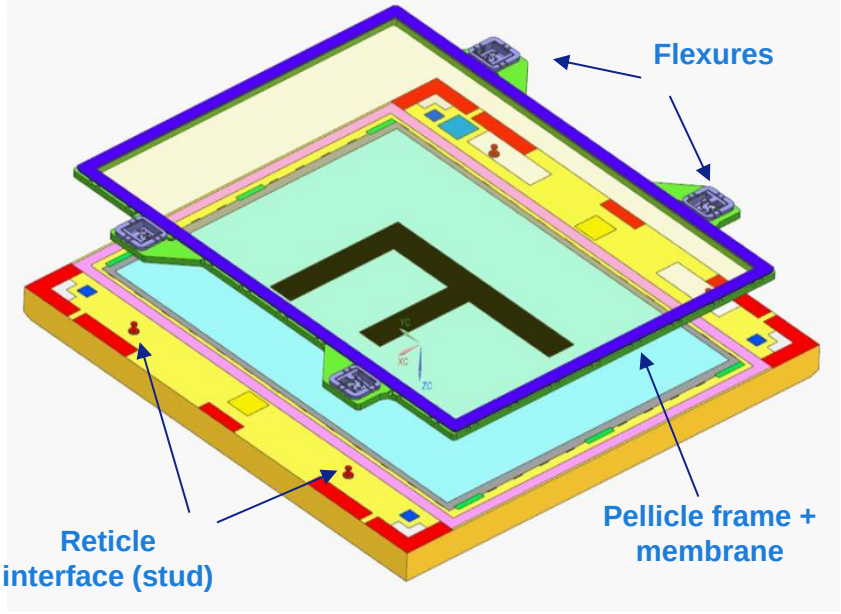
Key features

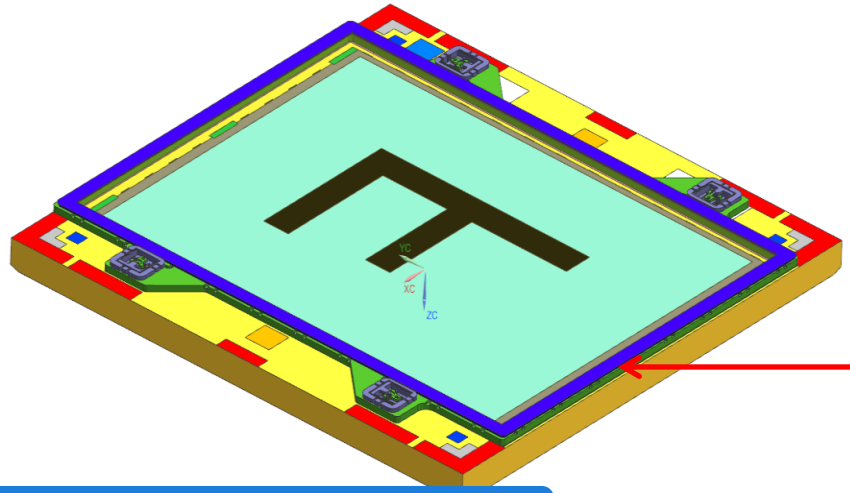
- Reticle front side defect-free solution
  - protects reticle front side from fall-on defects
  - particle free material combination and mounting technology to prevent particle generation
  - additional particle suppression towards pattern area
- Designed for use in NXE scanner
  - pump down/vent cycles compatible
  - vacuum and H_2 environment compatible
  - meets outgassing requirements
  - no overlay impact, distortion-free mounting
- Compatible with standard EUV mask flow
  - concept supports any type of pattern mask inspection: optical, e-beam, and actinic; both at mask shop and fab
  - allows for reticle repel cycle

Slide courtesy ASML. See Carmen Zoldesi “EUV pellicle development update” tomorrow in Session 10

Interchangeable NXE Pellicle concept

Allowing multiple inspection schemes





Key features

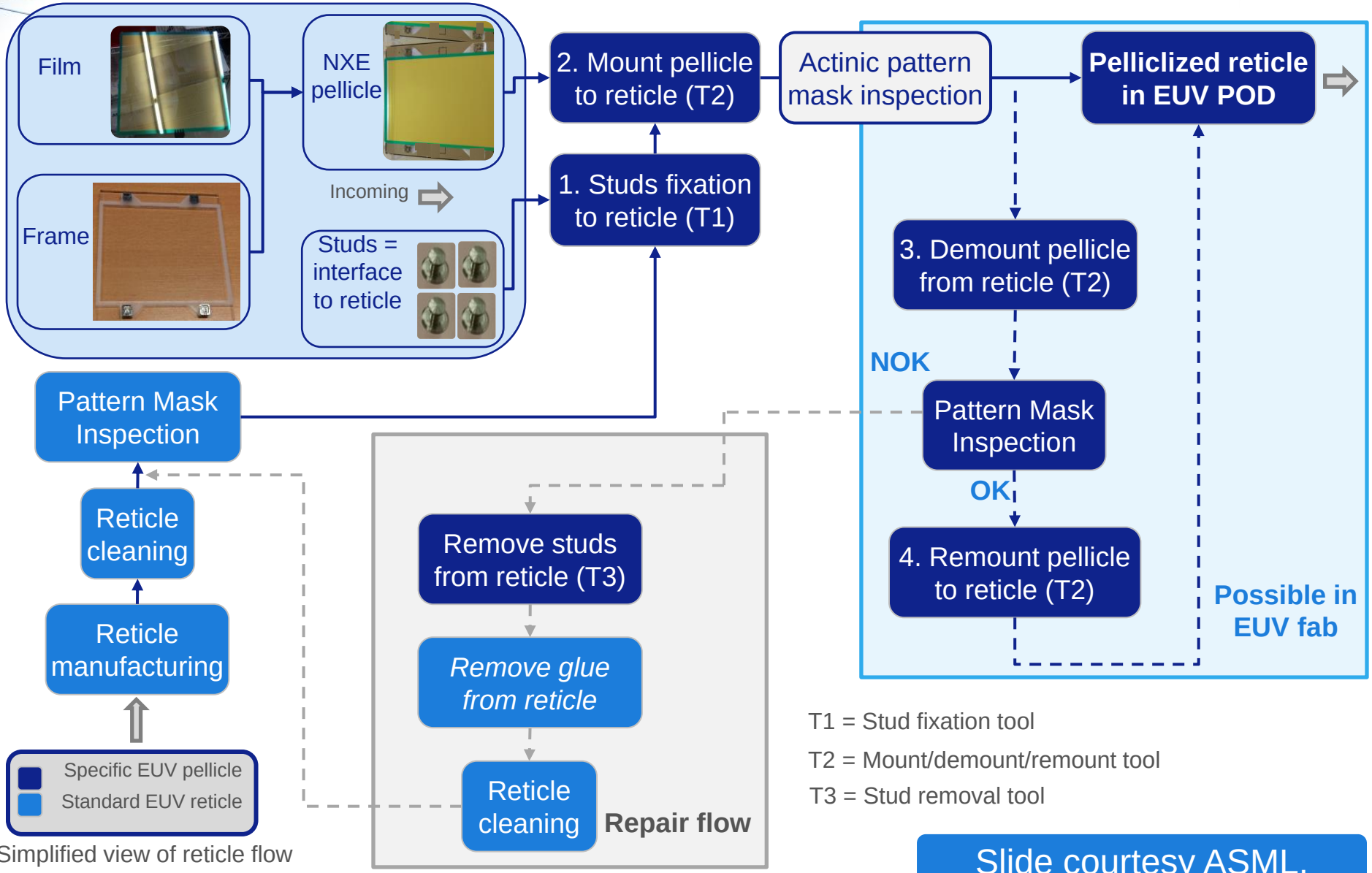
- Reticle front side defect-free solution
  - protects reticle front side from fall-on defects
  - particle free material combination and mounting technology to prevent particle generation
  - additional particle suppression towards pattern area
- Designed for use in NXE scanner
  - pump down/vent cycles compatible
  - vacuum and H_2 environment compatible
  - meets outgassing requirements
  - no overlay impact, distortion-free mounting
- Compatible with standard EUV mask flow
  - concept supports any type of pattern mask inspection: optical, e-beam, and actinic; both at mask shop and fab
  - allows for reticle repel cycle

1. Pellicle frame is not sealed. 200um gap needed for pump-down
2. ASML simulation predicts 1/200 attenuation of small particles
3. Critical to verify!

Slide courtesy ASML.

Interchangeable NXE pellicle concept

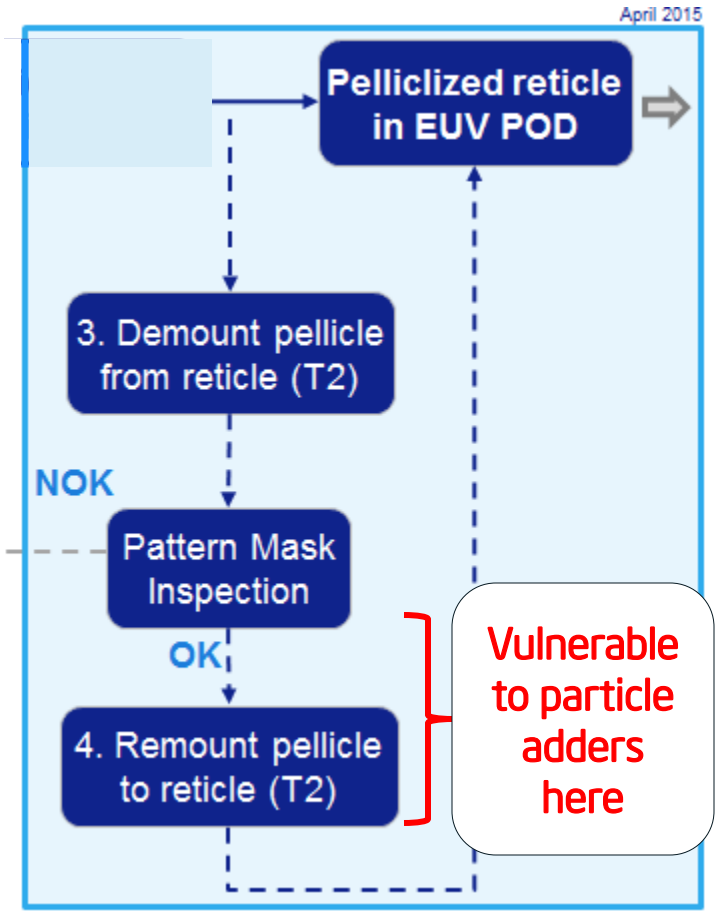
offers maximum flexibility to EUV mask shop back end and fab reticle flow



Simplified view of reticle flow

Slide courtesy ASML.

Pellicle removal for inspection



- Allows use of existing DUV inspection tools while pellicle is off
- Addresses tracking of PID growth (but at risk of adding particles)
- Could also use e-beam reticle inspection tool, but likely dirty
- Still vulnerable to undetected particles added between inspection and pellicle re-mount
- Any particles added will require removal of posts and reticle clean
- Likely desirable to integrate pellicle remove/replace into inspection tool to minimize time without pellicle protection

Pellicle summary

- Commitment by ASML to commercialize EUV pellicles is good news for EUV end-users
- Removable pellicle design is clever and impressively engineered
- Need to verify particle attenuation by 200um gap
- Does not eliminate need for post-pellicle mount/remount inspection
- Need industry engagement to integrate into mask tools and mask process flow
- Please get involved!

Conclusions

- Two years of solid progress on source power have debunked claims that EUVL can never achieve high productivity
- Availability, stability and operating cost are still concerns
- Complementary EUV/193i lithography requires continued improvements in both 193i and EUV masks
- Infrastructure (mostly mask-related) is in danger of limiting use of EUVL in HVM

Acknowledgements

Frank Abboud (Intel)
Yan Borodovsky (Intel)
Steve Carson (Intel)
Tim Crimmins (Intel)
Jeff Farnsworth (Intel)
Steve Johnston (Intel)
Sang Lee (Intel)
Ted Liang (Intel)
Brian McCool (Intel)
Rajesh Nagpal (Intel)
Shalesh Sampat (Intel)
Sam Sivakumar (Intel)
Eric Stenehjem (Intel)
Guojing Zhang (Intel)

Dan Smith (ASML)
Carmen Zoldesi (ASML)

Thanks to the following companies for supplying material in this presentation:

- AGC
- ASML
- Hoya
- Lasertec